

Product Overview

The NSI6801E is a single-channel isolated gate driver which is pin-compatible for popular opto-coupled gate driver. It can source and sink 5A peak current. System robustness is supported by 150kV/us minimum common-mode transient immunity (CMTI).

The driver operates with a maximum supply voltage of 32V. While the input circuit imitates the characters of LEDs, it has performance advantages compared to standard opto isolated gate drivers, including better reliability and aging performance, higher working temperature, shorter propagation delay and smaller pulse width distortion.

As a result, the NSI6801E is suitable to replace opto-isolated driver in high reliability, power density and efficiency switching power system.

Key Features

- Isolated single-channel driver
- Pin compatible, drop in upgrade for opto isolated gate drivers
- Driver side supply voltage: up to 32V with UVLO
- 5A peak source and sink output current
- High CMTI: $\pm 150\text{kV/us}$
- 75ns typical propagation delay
- 30ns maximum pulse width distortion
- Operation ambient temperature: $-40^{\circ}\text{C} \sim 125^{\circ}\text{C}$
- Lead-free component, suitable for lead-free soldering profile: 260°C , MSL3
- RoHS& REACH Qualified

Safety Regulatory Approvals

- UL recognition: 5700 V_{RMS} SOWW8 for 1 minute per UL1577
- DIN VDE V 0884-17:2017-01
- CSA component notice 5A

- CQC certification per GB4943.1-2022

Applications

- DC-to-AC solar inverters
- Motor drives
- UPS and battery chargers
- Isolated DC/DC and AC/DC power supplies

Device Information

Part Number	Spec difference	Package	Body Size
NSI6801EC-DSWWAR	12V	SOWW8	13.6×6.25×3.60mm

Functional Block Diagram

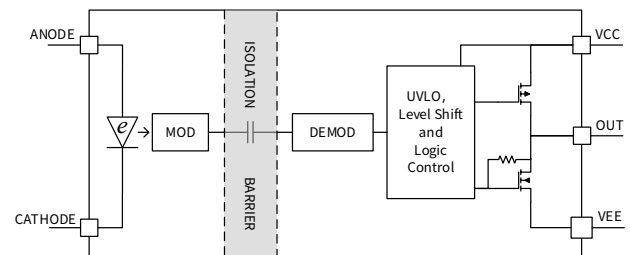


Figure 1. NSI6801E Block Diagram

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1. Pin Configuration and Functions

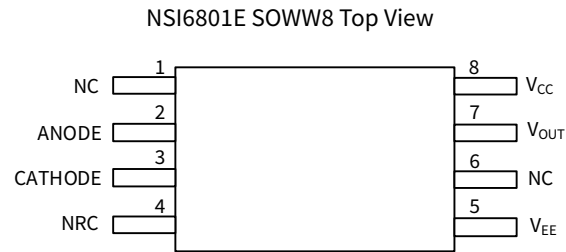


Table 1.1 NSI6801E Pin Configuration and Description

SYMBOL	PIN NO.	FUNCTION
ANODE	2	Anode of LED emulator
CATHODE	3	Cathode of LED emulator
V _{EE}	5	Negative output supply rail
V _{OUT}	7	Gate-drive output
V _{CC}	8	Positive output supply rail
NC	1,6	No Connection
NRC	4	Internally connected, not recommended connecting in circuit

2. Absolute Maximum Ratings

Parameters	Symbol	Min	Max	Unit
Average Input Current	I_{F_AVG}		25	mA
Peak Transient Input Current	I_{F_PEAK}		0.2	A
Reverse Input Voltage	V_{R_MAX}		6.5	V
Driver Side Supply Voltage	$V_{CC-V_{EE}}$	-0.3	38	V
Output Signal Voltage	V_{OUT}	$V_{EE}-0.3$	$V_{CC}+0.3$	V
Operating Junction Temperature	T_J	-40	150	°C
Storage Temperature	T_{stg}	-65	150	°C

3. ESD Ratings

	Ratings	Value	Unit
Electrostatic discharge	Human body model (HBM), per AEC-Q100-002-RevD ● All pins	±2000	V
	Charged device model (CDM), per AEC-Q100-011-RevB ● All pins	±1000	V

4. Recommended Operating Conditions

Parameters	Symbol	Min	Max	Unit
Input Current (ON)	$I_{F(ON)}$	7	16	mA
Input Voltage (OFF)	$V_{F(off)}$	-5.5	0.9	V
Driver Side Supply Voltage (NSI6801EC)	$V_{CC-V_{EE}}$	15	32	V
Driver Side Supply Voltage (NSI6801EB)	$V_{CC-V_{EE}}$	10	32	V
Ambient Temperature	T_A	-40	125	°C

5. Thermal Information

Parameters	Symbol	NSI6801E	Unit
Junction-to-ambient thermal resistance	$R_{\theta JA}$	70	°C/W
Junction-to-top characterization parameter	Ψ_{JT}	12.5	°C/W

6. Specifications

6.1. DC Electrical Characteristics

(Unless otherwise noted, Typical values are at $V_{CC}=15V$, $V_{EE}=GND$, $T_A=25^{\circ}C$. All min and max specifications are at $T_A=-40^{\circ}C$ to $125^{\circ}C$, $V_{CC}=15V$ to $32V$, $V_{EE}=GND$, $I_{F(ON)}=7mA$ to $16mA$, $V_{F(off)}=-5.5V$ to $0.9V$)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Driver Side Supply						
High Level Supply Current	I _{CCH}		1.7	3.5	mA	I _F =10mA, I _{OUT} =0mA
Low Level Supply Current	I _{CCL}		1.6	3.5	mA	V _F =0V, I _{OUT} =0mA
Driver Side Supply UVLO Threshold (NSI6801EC, 12V UVLO Level)						
VCC UVLO Rising Threshold	V _{CC_ON}	11.5	12.7	13.5	V	I _F =10mA
VCC UVLO Falling Threshold	V _{CC_OFF}	10.5	11.7	12.5	V	
VCC UVLO Hysteresis	V _{CC_HYS}		1.0		V	
Input Pin Characteristic						
Input Forward Threshold Current Low to High	I _{FLH}	1.5	2.8	4	mA	V _{OUT} >5V, C _g =1nF
Threshold Input Voltage High to Low	V _{FHL}	0.9			V	V _{OUT} <5V, C _g =1nF
Input Forward Voltage	V _F	1.8	2.1	2.4	V	I _F =10mA
Temp Coefficient of Input Forward Voltage	ΔV _F /ΔT		0.34		mV/°C	I _F =10mA
Input Capacitance	C _{IN}		17		pF	f=1MHz
Output Pin Characteristic						
High Level Output Voltage	V _{OH}	V _{CC} -0.3	V _{CC} -0.08		V	I _{OUT} =-50mA, I _F =10mA
Low Level Output Voltage	V _{OL}		40	65	mV	I _{OUT} =50mA, V _F =0V
High Level Peak Output Current	I _{OH}		5		A	V _{CC} =15V, pulse width<10μs
Low Level Peak Output Current	I _{OL}		5		A	V _{CC} =15V, pulse width<10μs

6.2. Switching Electrical Characteristics

(Unless otherwise noted, Typical values are at $V_{CC}=15V$, $V_{EE}=GND$, $T_A=25^{\circ}C$. All min and max specifications are at $T_J=-40^{\circ}C$ to $150^{\circ}C$, $V_{CC}=15V$ to $32V$, $V_{EE}=GND$, $I_{F(ON)}=7mA$ to $16mA$, $V_{F(off)}=-5.5V$ to $0.9V$)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Propagation Delay	t_{PLH}	50	75	100	ns	$C_{LOAD}=1nF$, $f=20kHz$ (50% Duty Cycle)
Propagation Delay	t_{PHL}	50	69	100	ns	
Pulse Width Distortion $ t_{PLH}-t_{PHL} $	t_{PWD}		6	30	ns	
Propagation Delay Difference Between Any Two Parts ($t_{PHL}-t_{PLH}$) ⁽¹⁾	PDD	-35		35	ns	
Output Rise Time (20% to 80%)	t_R		13	20	ns	
Output Fall Time (80% to 20%)	t_F		13	20	ns	
Common Mode Transient Immunity	CMTI	150			kV/ μs	Verified by design

(1) The difference between t_{PHL} and t_{PLH} between any two parts under the same test condition, ensured by characterization.

6.3. Typical Performance characteristics(TBD)

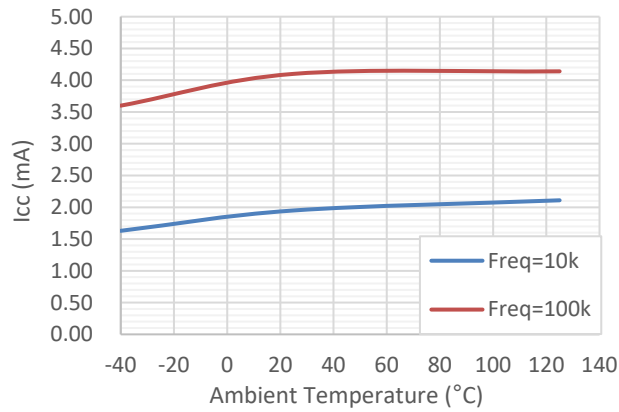


Figure 6.1 Supply currents versus Temperature

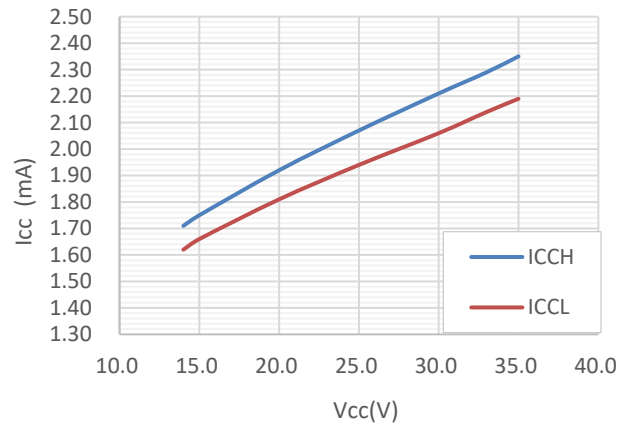


Figure 6.2 Supply current versus Supply Voltage

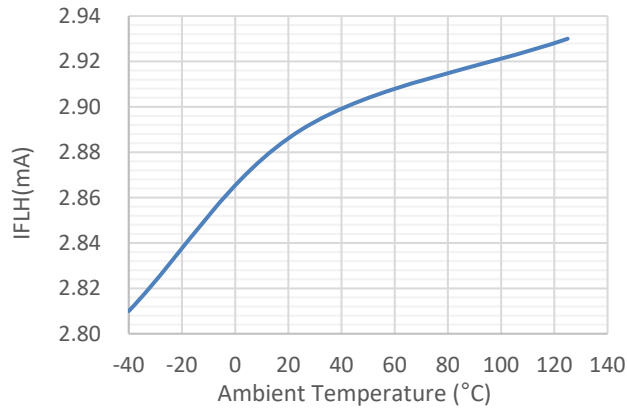


Figure 6.3 Forward threshold current versus Temperature

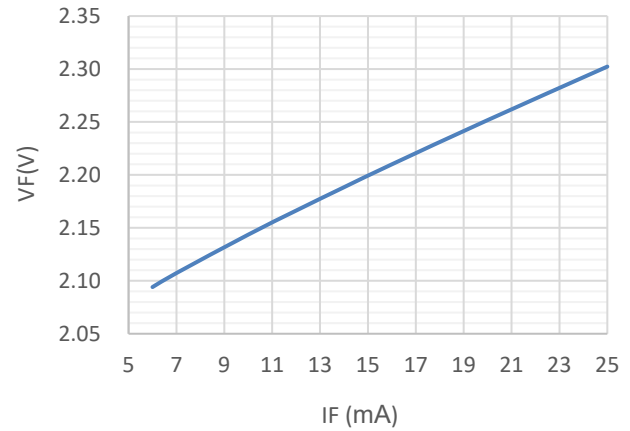


Figure 6.4 Forward current versus Forward voltage drop

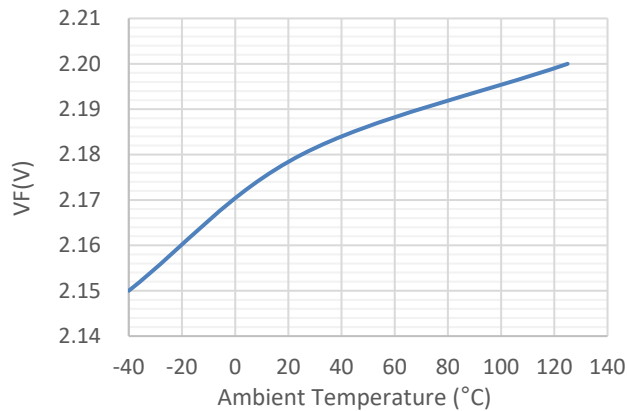


Figure 6.5 Forward voltage drop versus Temperature

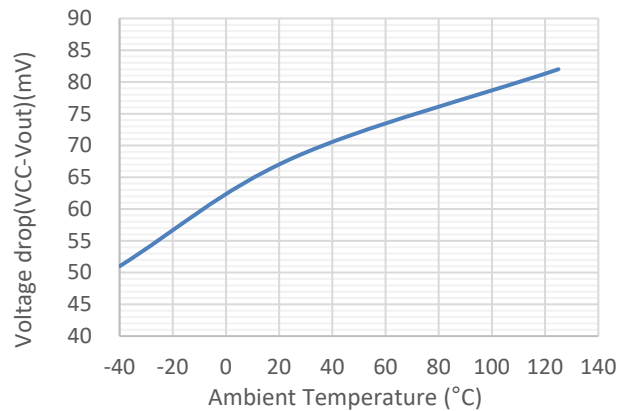


Figure 6.6 V_{OH} (50mA Load) versus Temperature

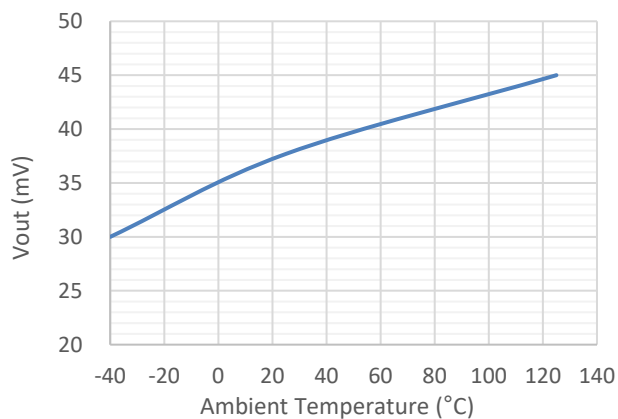


Figure 6.7 V_{OL} versus Temperature

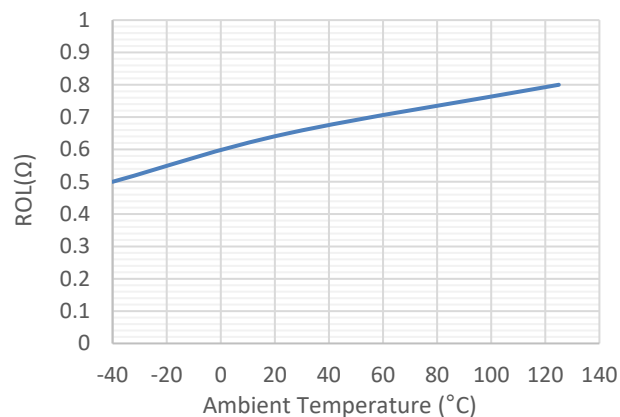


Figure 6.18 R_{OL} versus Supply voltage

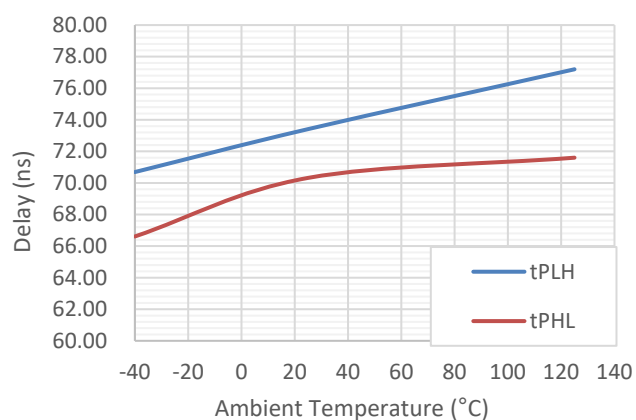


Figure 6.9 Propagation delay versus Temperature

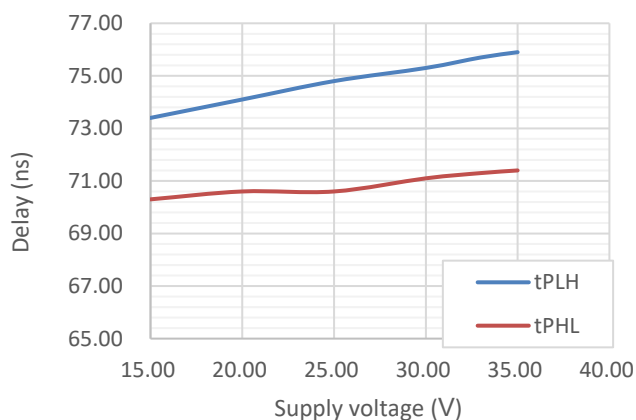


Figure 6.10 Propagation delay versus Supply voltage

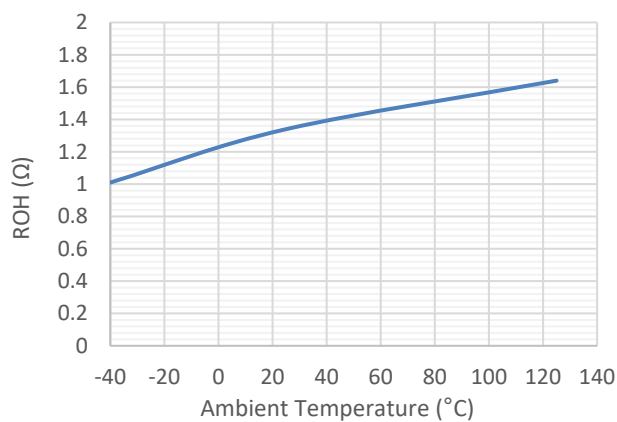


Figure 6.11 R_{OH} versus Temperature

6.4. Parameter Measurement Information

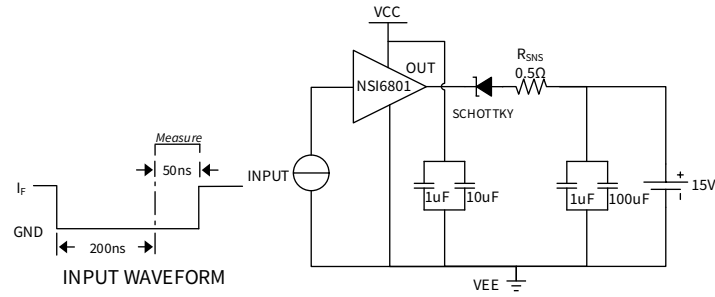


Figure 6.12 I_{OL} Sink Current Test Circuit

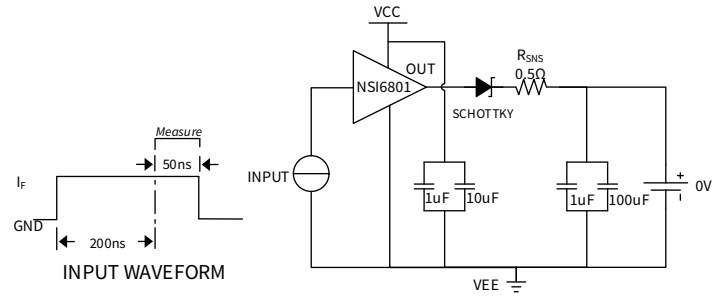


Figure 6.13 I_{OH} Source Current Test Circuit

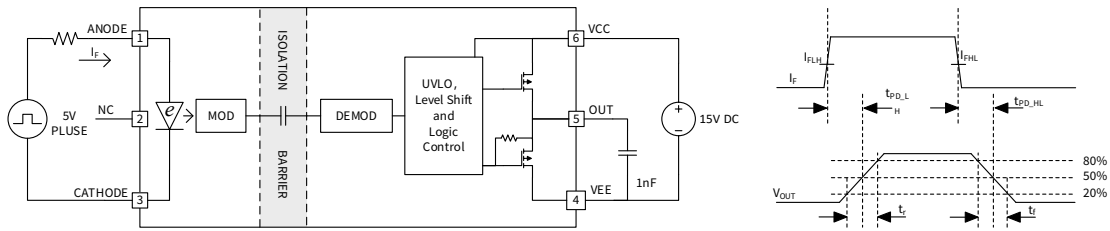


Figure 6.14 I_F to V_{OUT} Propagation Delay, Rise Time and Fall Time

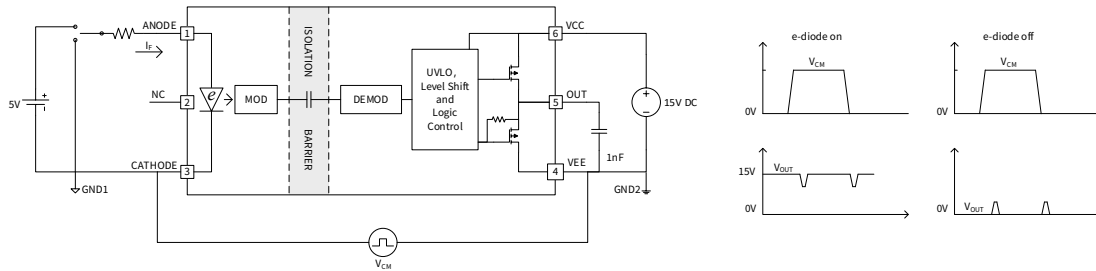


Figure 6.15 Common Mode Transient Immunity Test Circuit

7. High Voltage Feature Description

7.1. Insulation and Safety Related Specifications

Parameters	Symbol	Value	Unit	Comments
Minimum External Air Gap (Clearance)	CLR	15	mm	Shortest terminal-to-terminal distance through air
Minimum External Tracking (Creepage)	CPG	15	mm	Shortest terminal-to-terminal distance across the package surface
Distance Through Insulation	DTI	28	μm	internal gap
Tracking Resistance (Comparative Tracking Index)	CTI	600	V	DIN EN 60112 (VDE 0303-11); IEC 60112
Material Group		I		IEC 60664-1

7.2. Insulation Characteristics for SOWW8 Package

Description	Test Condition	Symbol	Value	Unit
Overvoltage Category per IEC60664-1	For Rated Mains Voltage $\leq 600V_{RMS}$		I to IV	
	For Rated Mains Voltage $\leq 1000V_{RMS}$		I to III	
Climatic Category			40/125/21	
Pollution Degree	per DIN VDE 0110, Table 1		2	
Maximum Working Isolation Voltage	AC voltage	V_{IOWM}	1500	V_{RMS}
	DC voltage		2121	V_{DC}
Maximum Repetitive Peak Isolation Voltage		V_{IORM}	2121	V_{PEAK}
Apparent Charge	Method B ,routine test(100% production) and preconditioning (type test); $V_{ini}=1.2*V_{IOTM}$, $V_{pd(m)}=V_{IORM}\times 1.875$, $t_{ini}=t_m=1s$	q_{pd}	<5	pC
	Method A, after Environmental Tests Subgroup 1, $V_{pd(m)}=V_{IORM}\times 1.6$, $t_{ini}=60s$, $t_m=10s$			pC
	Method A,after Input and Output Safety Test Subgroup 2 and Subgroup 3, $V_{pd(m)}=V_{IORM}\times 1.2$, $t_{ini}=60s$, $t_m=10s$			pC
Maximum Transient Isolation Voltage	$t = 60s$	V_{IOTM}	8000	V_{PEAK}
Maximun Impulse Voltage	Tested in air, 1.2/50 μs waveform per IEC62368-1	V_{IMP}	6000	V_{PEAK}
Maximum Surge Isolation Voltage	Test method per IEC62368-1, 1.2/50 μs waveform, $V_{IOSM}\geq V_{IMP}\times 1.3$	V_{IOSM}	10000	V_{PEAK}
Isolation Resistance	$V_{IO}=500V$ at $T_A=T_S=25^{\circ}C$	R_{IO}	$>10^{12}$	Ω
	$V_{IO}=500V$ at $T_A=T_S=150^{\circ}C$		$>10^9$	Ω
	$V_{IO}=500V$ at $100^{\circ}C\leq T_A\leq 125^{\circ}C$		$>10^{11}$	Ω
Isolation Capacitance	$f = 1MHz$	C_{IO}	1	pF
Insulation Specification per UL1577				
Withstand Isolation Voltage	$V_{TEST} = 1.2 \times V_{ISO}$, $t=1s$,100% production test	V_{ISO}	5700	V_{RMS}

7.3. Safety-Limiting Values for SOWW8 Package

Description	Test Condition	Symbol	Value	Unit
Maximum Safety Temperature		T_s	150	°C
Safety Input, Output, or Total Power	$R_{\theta JA}=70^{\circ}\text{C/W}$, $T_J=150^{\circ}\text{C}$, $T_A=25^{\circ}\text{C}$	P_s	1.79	W
Safety Input, Output, or Supply Current	$R_{\theta JA}=70^{\circ}\text{C/W}$, $V_{CC}=15\text{V}$, $T_J=150^{\circ}\text{C}$, $T_A=25^{\circ}\text{C}$	I_s	119	mA
	$R_{\theta JA}=70^{\circ}\text{C/W}$, $V_{CC}=30\text{V}$, $T_J=150^{\circ}\text{C}$, $T_A=25^{\circ}\text{C}$	I_s	59.5	mA

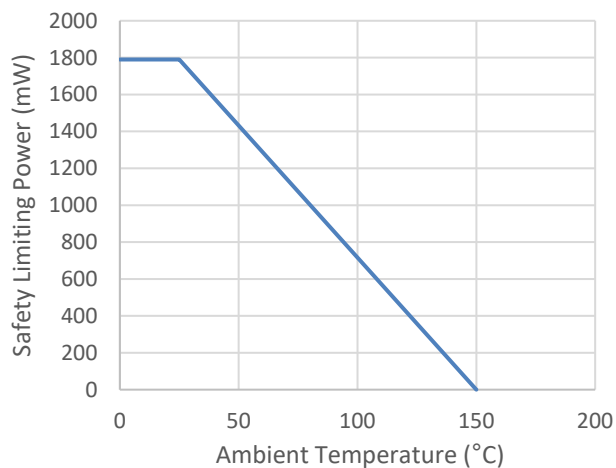


Figure 7.1 Thermal Derating Curve for Limiting Power per DIN VDE V 0884-17

7.4. Regulatory Information for SOWW8 Package

UL		VDE	CQC
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	Certified according to DIN EN IEC 60747-17(VDE 0884-17)	Certified by CQC11-471543-2012 GB4943.1-2022
Single Protection, 5700V _{RMS} Isolation Voltage	Single Protection, 5700V _{RMS} Isolation voltage	Reinforced Insulation V _{IORM} =2121V _{PEAK} , V _{IOTM} =8000V _{PEAK} , V _{IOSM} =10000V _{PEAK}	Reinforced Insulation
Pending		Pending	Pending

8. Function Description

The NSI6801E is a single-channel isolated gate driver that is pin-compatible with popular opto-coupled gate driver. The integrated galvanic isolation between control input logic and driving output stage grants additional safety. The device can source and sink 5A peak current, making it suitable for driving IGBTs, power MOSFETs and SiC MOSFETs in various applications such as motor control systems, solar inverters and power supplies.

8.1. Functional Block Diagram

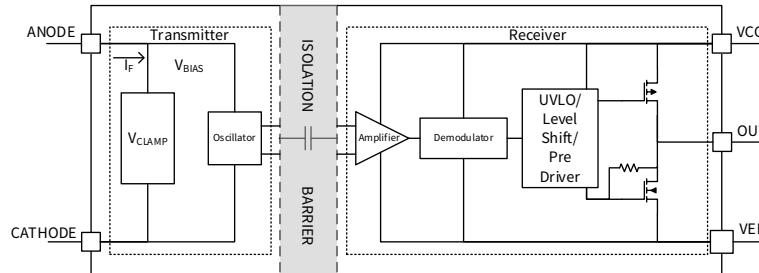


Figure 8.1 NSI6801E Functional Block Diagram

8.2. Truth Tables

Table 8.1 Driver Function Table ⁽¹⁾

<i>e-diode</i>	<i>V_{CC} status</i>	<i>Outputs</i>
X	Powered Down	L
$I_F > I_{FLH}$	Powered Up	H
$V_F < V_{FHL}$	Powered Up	L

(1) H= Logic High; L= Logic Low; X= Irrelevant

8.3. Output Stage

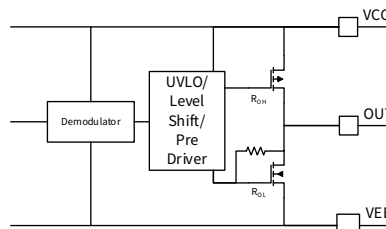


Figure 8.2 NSI6801E Output Stage

Table 8.2 NSI6801E Output Stage On-Resistance

<i>R_{OH}</i>	<i>R_{OL}</i>	<i>Unit</i>
1.4	0.8	Ω

The NSI6801E has P-channel MOSFET to pull up the OUT pin when turning on external power transistor. The measurement result R_{OH} represents the on-resistance of P-channel MOSFET. The equivalent pull-up resistance of NSI6801E is R_{OH} . The result is quite small, indicating the strong driving capability of NSI6801E.

The pull-down structure of NSI6801E is simply composed of an N-channel MOSFET with on-resistance of R_{OL} . The result is quite small, indicating the strong driving capability of NSI6801E.

8.4. V_{CC} and Under Voltage Lock Out (UVLO)

The lower limit of the driver side supply voltage (V_{CC}) is determined by the internal UVLO protection feature of the device. V_{CC} voltage

should not fall below the UVLO threshold for normal operation, or else the gate-driver outputs can become clamped low.

A local bypass capacitor should be placed between the V_{CC} and V_{EE} pins, with a value of 220nF to 10 μ F for device biasing. An additional 100nF capacitor in parallel with the device biasing capacitor is recommended for high frequency filtering. Both capacitors should be positioned as close to the device as possible. Low-ESR, ceramic surface-mount capacitors are recommended.

8.5. Active Pull-Down

The Active Pull-Down feature ensures a safe IGBT or MOSFET off-state if V_{CC} is not connected to the power supply. When V_{CC} is floating, the driver output is held low and clamping V_{OUT} pin to approximately 1.9V higher than V_{EE} .

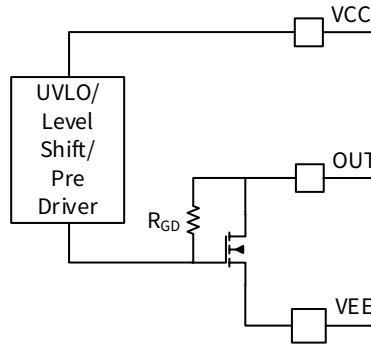


Figure 8.3 Active pulldown

8.6. Short Circuit Clamping

During short circuit the gate voltage of IGBT or MOSFET tends to rise because of the feedback via the Miller capacitance. The diode between V_{OUT} and V_{CC} pins inside the driver limits this voltage to a value slightly higher than the supply voltage. A maximum current of 500mA may be fed back to the supply through this path for 10 μ s. If higher currents are expected or tighter clamping is desired external Schottky diodes may be added.

9. Application Note

9.1. Typical Application

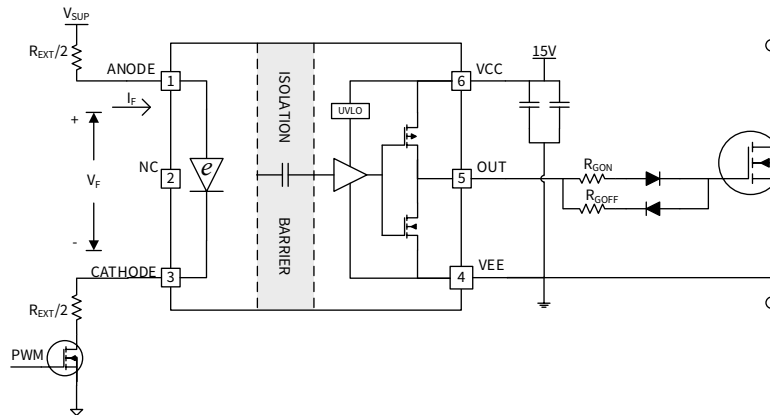


Figure 9.1 NSI6801E typical application circuit with NMOS driving input stage

Bypassing capacitors connecting between V_{CC} and V_{EE} are needed to achieve reliable performance. To filter noise, 0.1 μ F/50V ceramic capacitor is recommended to place as close as possible to NSI6801E. To support high peak currents when turning on external power transistor, additional 10 μ F/50V ceramic capacitor is recommended. If the V_{CC} power supply is located long distance from the IC, bigger capacitance is needed.

NSI6801E requires 7mA to 16mA bias current that flows into the e-diode for normal operation. The PWM from MCU is not suitable to provide such current directly and external circuit is needed. In Figure 9.1, one NMOS is used with split input resistors. Another input drive method is using one buffer, as shown in Figure 9.2. The details to calculate input drive parameters are in Chapter 9.3.

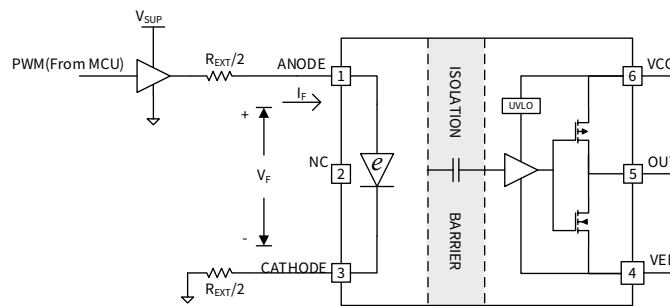


Figure 9.2 NSI6801E typical application circuit with one buffer driving input stage

9.2. Interlock Protection

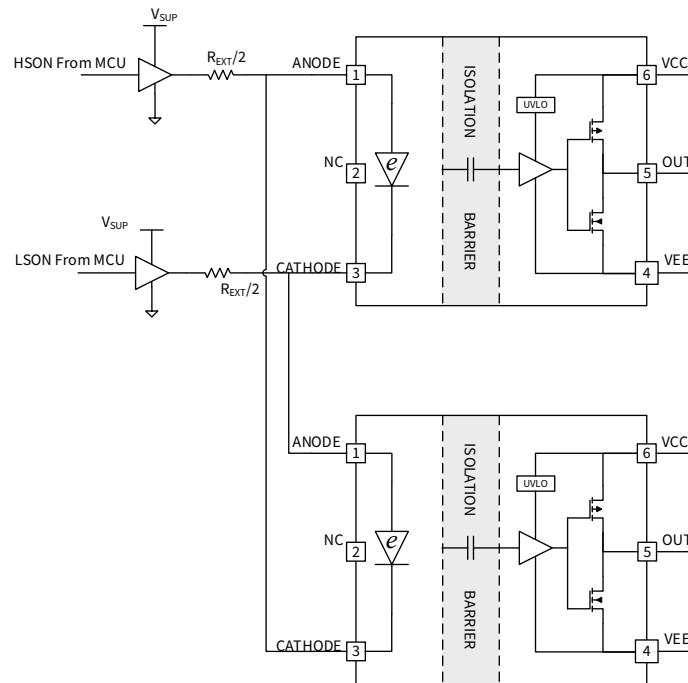


Figure 9.3 Interlock Protection using NSI6801E

For applications to drive power transistors in half bridge configuration, two NSI6801E can be used. Interlock protection is possible as shown in Figure 9.3. If the controller has some mistake, leading to negative dead time, the output PWM of NSI6801E is adjusted to avoid power transistor shoot through. The input side reverse breakdown voltage of NSI6801E is greater than 6.5V, which supports interlock protection of 3.3V or 5V PWM signal source.

9.3. Selecting Input Resistor

The recommended forward current range for NSI6801E is 7mA to 16mA. The value of input resistor, buffer supply voltage and buffer internal resistance influence the forward current, as shown in Equation (1). In Figure 9.1, R_{IN1} is the on-resistance of the external NMOS. In Figure 9.2, R_{IN2} is the buffer output impedance in output “High” state. In Figure 9.3, R_{IN3} is the summary of buffer output impedance in “High” and “Low” state.

$$R_{EXT} = \frac{V_{SUP} - V_F}{I_F} - R_{INx} \quad (1)$$

The parameter variation needs to be taken into consideration when selecting input resistor. Table 9.1 lists parameter variation in this example. Manufacturer’s tolerance for R_{EXT} is 2%.

Table 9.1 External parameters range when calculating input resistor

Parameters	Min	Typ	Max
NSI6801E forward current I_F	7mA	10mA	16mA
NSI6801E forward voltage V_F	1.8V	2.1V	2.4V
Buffer supply voltage V_{SUP}	5V*95%	5V	5V*105%
R_{IN1}	0.25Ω	/	1Ω
R_{IN2}	13Ω	18Ω	22Ω

R_{IN3}	9Ω	14Ω	18Ω
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R_{EXT} calculated based on these parameters above is as follows:

$$R_{EXT_min} = \left(\frac{V_{SUP_max} - V_{F_min}}{I_{F_max}} - R_{INx_min} \right) / (1 - 2\%) \quad (2)$$

$$R_{EXT_typ} = \frac{V_{SUP_typ} - V_{F_typ}}{I_{F_typ}} - R_{INx_typ} \quad (3)$$

$$R_{EXT_max} = \left(\frac{V_{SUP_min} - V_{F_max}}{I_{F_min}} - R_{INx_max} \right) / (1 + 2\%) \quad (4)$$

Where $R_{INx} = R_{IN1}$ or R_{IN2} or R_{IN3} is determined by topology.

9.4. PCB Layout

Careful PCB layout is essential for optimal performance. Some key guidelines are:

- The bypass capacitors should be placed close to NSI6801E, between V_{CC} to V_{EE} .
- There is high switching current that charges and discharges the gate of external power transistor, leading to EMI and ring issues. The parasitic inductance of this loop should be minimized, by decreasing loop area and place NSI6801E close to power transistor.
- Place large amount of copper connecting to V_{EE} pin and V_{CC} pin for thermal dissipation, with priority on V_{EE} pin. If the system has multi V_{EE} or V_{CC} layers, use multiple vias of adequate size for connection.

To ensure isolation performance between primary and secondary side, the space under the chip should keep free from planes, traces, pads or via.

10. Package Information

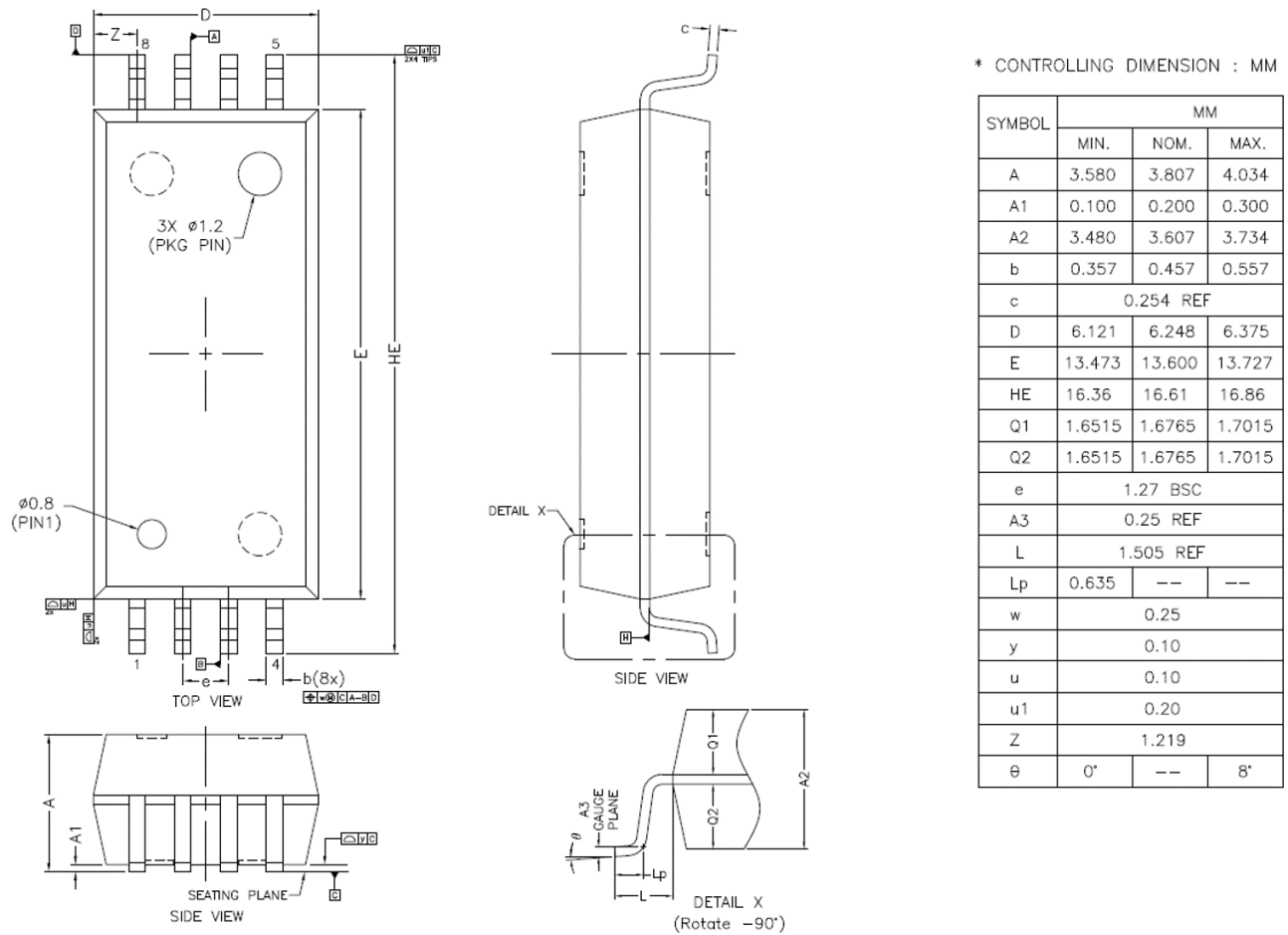


Figure 10.1 SOWW8 Package Shape and Dimension in millimeters

11. Ordering Information

Part Number	Isolation Rating (kV)	UVLO Level	Vout Connection	Temperature	MSL	Package Drawing	SPQ	Category
NSI6801EC-DSWWAR	5700	12V	Pin 7	-40 to 125°C	3	SOWW8	1000	Industrial

12. Documentation Support

Part Number	Product Folder	Datasheet	Technical Documents	Isolated Driver Selection Guide
NSI6801	Click here	Click here	Click here	Click here

13. Tape and Reel Information

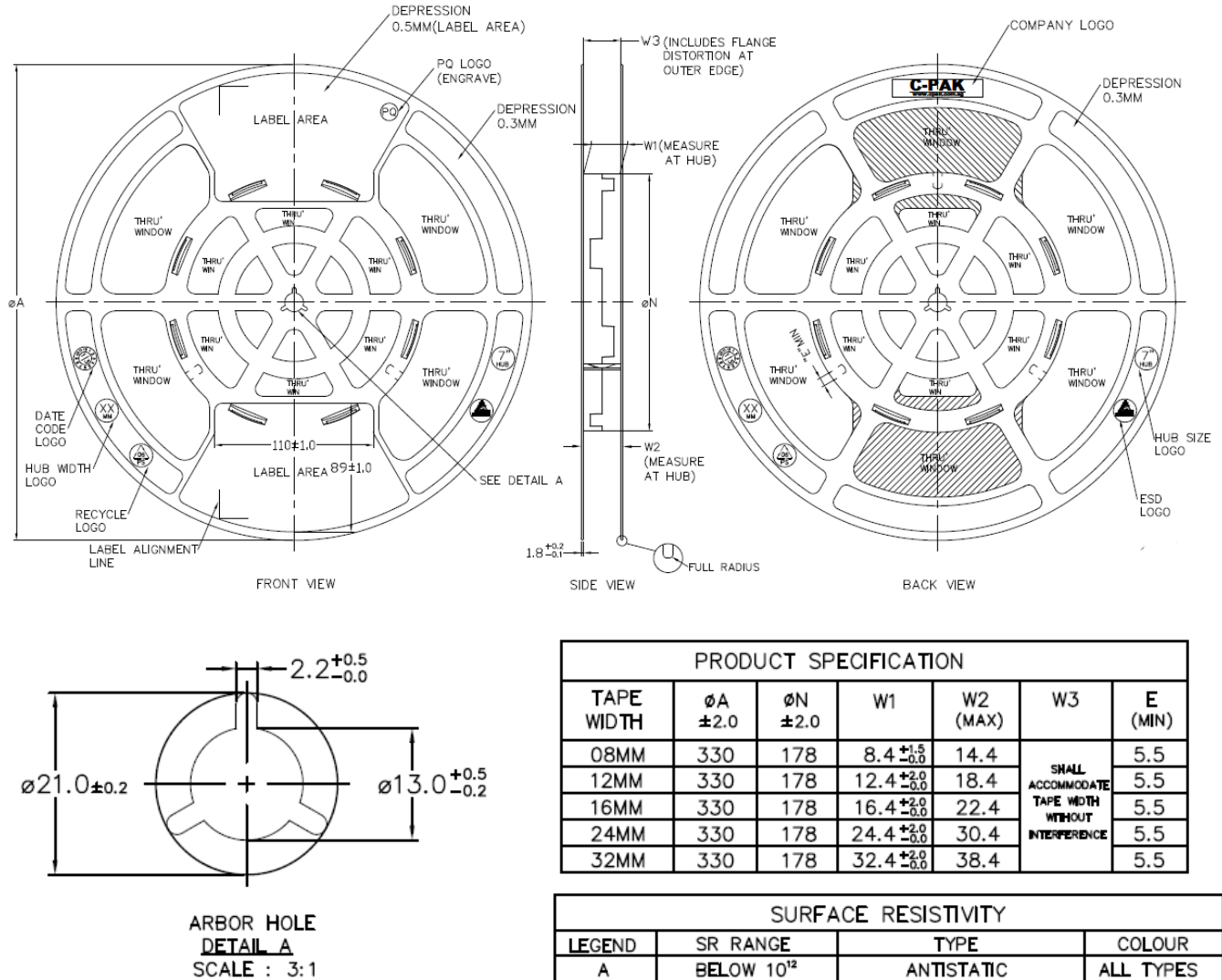


Figure 13.1 Reel Information

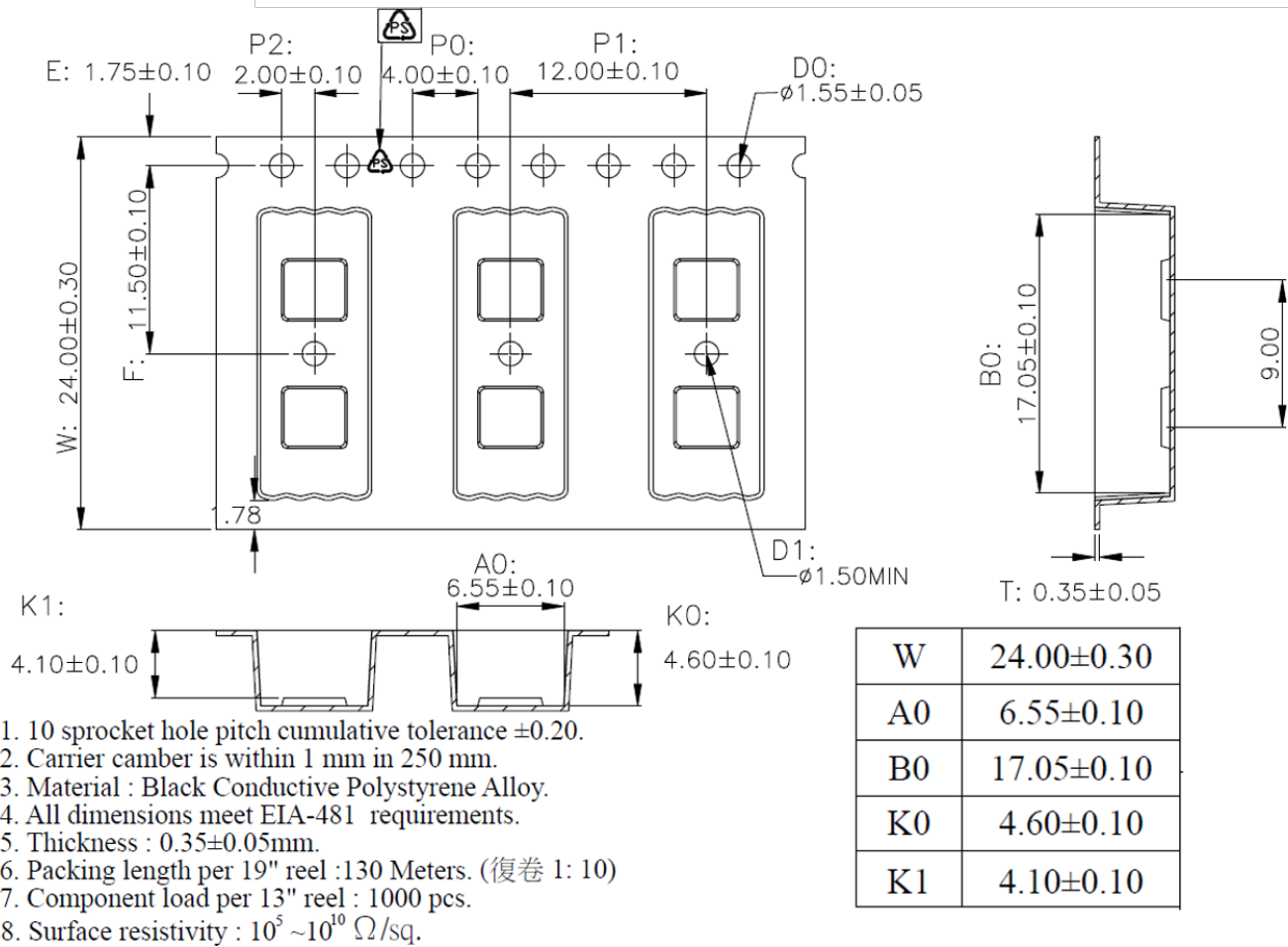


Figure 13.2 Tape Information of SOWW8

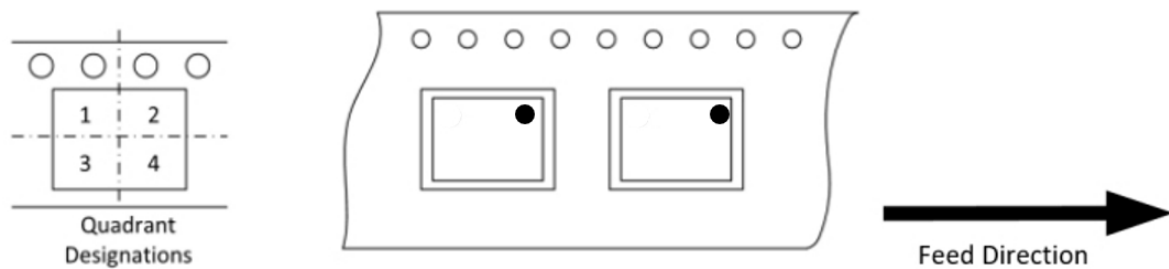


Figure 13.3 Quadrant Designation for Pin1 Orientation in Tape

14. Revision History

Revision	Description	Date
1.0	Initial version	2024/12/1

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